TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX07F,TC74LCX07FT,TC74LCX07FK

Low-Voltage HEX Buffer with 5-V Tolerant Inputs and Outputs (open drain)

The TC74LCX07 is a high-performance CMOS buffer. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The TC74LCX07 has high performance MOS N-channel transistor. (open-drain outputs)

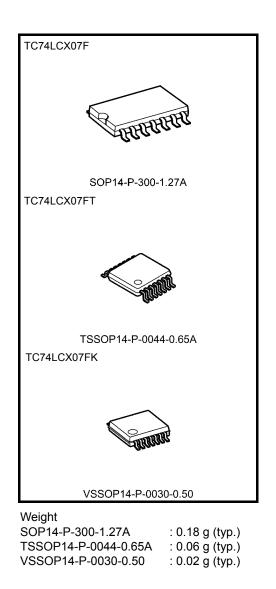
The device is designed for low-voltage $(3.3 \text{ V}) \text{ V}_{CC}$ applications, but it could be used to interface to 5-V supply* environment for inputs.

All inputs are equipped with protection circuits against static discharge.

*IOUT absolute maximum rating must be observed.

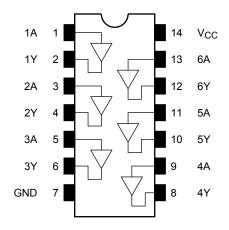
Features

- Low-voltage operation: $V_{CC} = 1.65$ to 5.5 V
- High-speed operation: $t_{pz} = 3.7 \text{ ns} (max) (V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$
- Output current: $I_{OL} = 24 \text{ mA} (min) (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: > -500 mA
- Available in JEITA SOP, TSSOP and VSSOP (US)
- Open-drain outputs
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 07 type



Note: The Voltage operation of V_{CC} =1.65 to 5.5V is only applicable for products which manufactured from January 2009 onward.

Pin Assignment (top view)



Truth Table

Inputs	Outputs
A	Y
L	L
Н	Z

Z: High impedance

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	–0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC output voltage	V _{OUT}	-0.5 to 7.0 (Note 2)	V
Input diode current	IIK	-50	mA
Output diode current	I _{OK}	–50 (Note 3)	mA
DC output current	IOUT	50	mA
Power dissipation	PD	180	mW
DC V _{CC} /ground current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	–65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

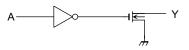
Note 2: Output in OFF state. IOUT absolute maximum rating must be observed (Output in low state)

Note 3: $V_{OUT} < GND$

IEC Logic Symbol

4.4	1	1 . ^	2 1Y
1A -	3	<u>1 v</u>	4
2A -	5		
3A -	9		<u> </u>
4A -	11		10 4Y
5A -	13		10 12 5Y
6A -			

Systm Diagram (per gate)



Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	1.65 to 5.5	V
Tower supply voltage	vcc	1.5 to 5.5 (Note 2)	v
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to 5.5	V
		32 (Note 3)	
Output current	I _{OL}	24 (Note 4)	mA
		12 (Note 5)	
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 6)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: $V_{CC} = 4.5$ to 5.5 V

Note 4: $V_{CC} = 3.0$ to 3.6 V

Note 5: $V_{CC} = 2.7$ to 3.0 V

Note 6: $V_{CC} = 1.65$ to 5.5 V

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics Symbol Test Condition		andition		Min Max		Unit						
Characte	1151105	Symbol	Test Condition		V _{CC} (V)	IVIIII	IVIAX	Offic				
						Vcc × 0.9						
					2.3 to 2.7	1.7	_					
	H-level	VIH		_	2.7 to 3.6	2.0						
Input voltage					4.5 to 5.5	Vcc × 0.7	_	v				
					1.65 to 2.3	_	Vcc × 0.1					
	L-level	VIL			2.3 to 2.7		0.7					
	L-IEVEI	۷IL		—	2.7 to 3.6		0.8					
						—	Vcc × 0.3					
				I _{OL} = 100 μA	1.65 to 5.5	—	0.2					
			$V_{IN} = V_{IL}$	$I_{OL} = 4 \text{ mA}$	1.65	—	0.45					
				I _{OL} = 8 mA	2.3	_	0.7					
Output voltage	L-level	V _{OL}		$V_{IN} = V_{IL}$	$V_{IN}=V_{IL}$	$V_{IN} = V_{IL}$	$V_{IN} = V_{IL}$	$I_{OL} = 12 \text{ mA}$	2.7	_	0.4	V
							I _{OL} = 16 mA	3.0	—	0.4		
				I _{OL} = 24 mA	3.0	—	0.55					
				$I_{OL} = 32 \text{ mA}$	4.5	_	0.55					
Input leakage current	t	I _{IN}	V _{IN} = 0 to 5.5 V		1.65 to 5.5	_	±5.0	μA				
Output OFF state cur	rrent	I _{OZ}	$V_{IN} = V_{IH}$, $V_{OUT} = 0$ to 5.5 V		1.65 to 5.5	_	±5.0	μA				
Power-off leakage cu	ırrent	I _{OFF}	$V_{IN}/V_{OUT} = 5.5 V$		0	_	10.0	μA				
Quiescent supply cur	rrent	ICC	V _{IN} = V _{CC} or GND		1.65 to 5.5	—	10.0	μA				
Increase in Icc per in	put	Alee			2.7 to 3.6	—	500	μΑ				
increase in icc per in	put	ΔI _{CC}	$V_{IH} = V_{CC} - 0.6$	v	4.5 to 5.5	—	1	mA				

AC Characteristics (Ta = -40 to 85°C)

Characteristics Symbol Test Condition		Test Condition		Min	Max	Unit
	Cymbol		$V_{CC}(V)$		Max	Onit
			1.8 ± 0.15	1.5	22.0	
			$\textbf{2.5}\pm\textbf{0.2}$	1.2	11.0	
Output enable time	t _{pZL}	Figure 1, Figure 2	2.7	1.0	4.4	ns
			$\textbf{3.3}\pm\textbf{0.3}$	0.8	3.7	
			5.0 ± 0.5	0.5	3.0	
		Figure 1, Figure 2	1.8 ± 0.15	1.5	22.0	
			2.5 ± 0.2	1.2	11.0	
Output disable time	t _{pLZ}		2.7	1.0	4.4	ns
			3.3 ± 0.3	0.8	3.7	
			5.0 ± 0.5	0.5	3.0	
Output to output skew	tosZL	(Noto)	2.7	_	_	ne
	IUSZL	(Note)	$\textbf{3.3}\pm\textbf{0.3}$		1.0	ns

Note: Parameter guaranteed by design. $(t_{osZL} = |t_{pZLm} - t_{pZLn}|)$

Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 2.5 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Quiet output maximum dynamic V _{OL}	VOLP	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V
Quiet output minimum dynamic V_{OL}	V _{OLV}	$V_{IH} = 3.3 V, V_{IL} = 0 V$	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	1	V _{CC} (V)	Тур.	Unit
Input capacitance	C _{IN}			3.3	7	pF
Output capacitance	C _{OUT}			3.3	8	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (I	Note)	3.3	5	pF

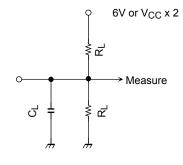
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per gate)

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AC Test Circuit



Parameter		Switch
	6.0 V	@ V _{CC} =3.3 \pm 0.3 V
		@ V _{CC} =2.7V
t _{pLZ} , t _{pZL}	$V_{CC} \times 2$	@ V_CC=5.0 \pm 0.5 V
		@ V _{CC} =2.5 \pm 0.2V
		@ V_CC=1.8 \pm 0.15 V

Figure 1

AC Waveform

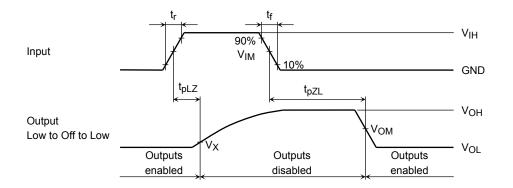


Figure 2 t_{pLZ}, t_{pZL}

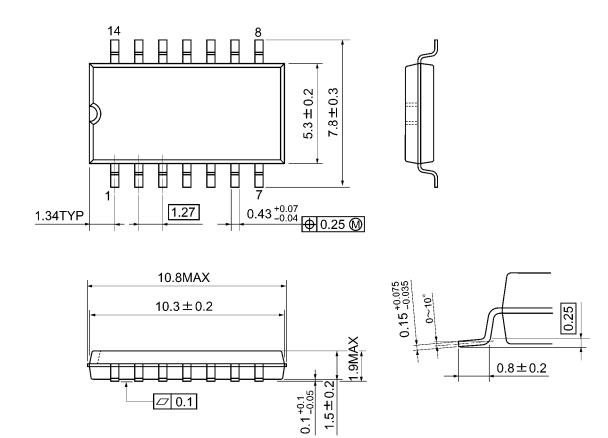
		V _{CC}					
	Symbol	$5.0\pm0.5\;V$	$\begin{array}{c} 3.3\pm0.3~\text{V}\\ 2.7\text{V} \end{array}$	$2.5\pm0.2~V$	$1.8\pm0.15~\text{V}$		
Input	VIH	V _{CC}	2.7V	V _{CC}	V _{CC}		
	VIM	V _{CC} /2	1.5V	V _{CC} /2	V _{CC} /2		
	tr,tf	2.5ns	2.5ns	2.0ns	2.0ns		
Output	V _{OM}	V _{CC} /2	1.5V	V _{OH} /2	V _{OH} /2		
	VX	V _{OL} +0.3V	V _{OL} +0.3V	V _{OL} +0.15V	V _{OL} +0.15V		
Load	CL	50pF	50pF	30pF	30pF		
	RL	500 Ω	500 Ω	500 Ω	1kΩ		



Package Dimensions

SOP14-P-300-1.27A

Unit: mm

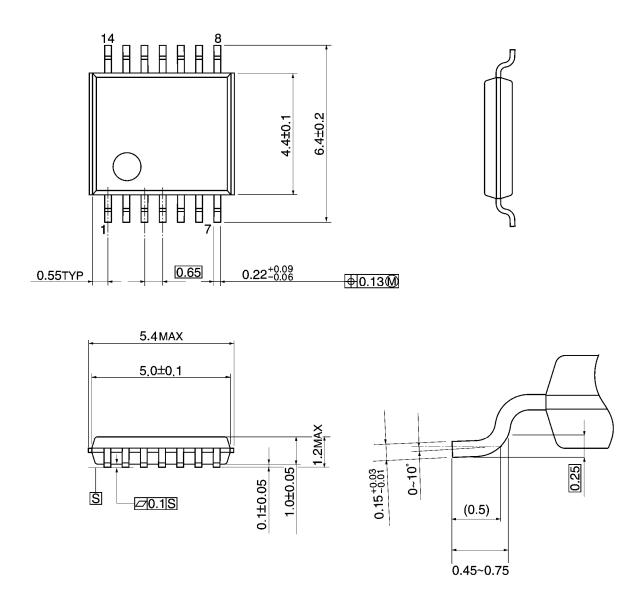


Weight: 0.18 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm



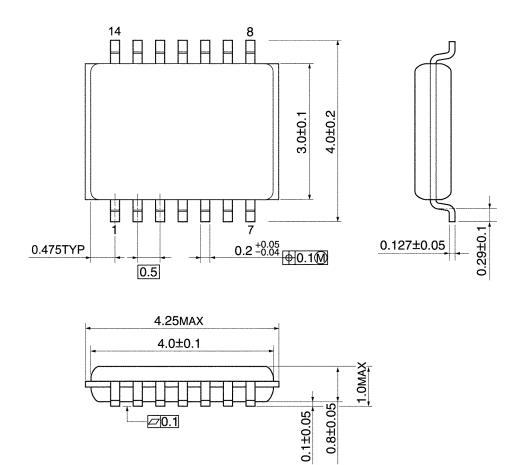
Weight: 0.06 g (typ.)



Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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